

Experimentally Observed Electrical Durability of 4H-SiC JFET ICs Operating from 500 °C to 700 °C

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Abstract. Prolonged 500 °C to 700 °C electrical testing data from 4H-SiC junction field effect transistor (JFET) integrated circuits (ICs) are combined with post-testing microscopic studies in order to gain more comprehensive understanding of the durability limits of the present version of NASA Glenn's extreme temperature microelectronics technology. The results of this study support the hypothesis that $T \geq 500$ °C durability-limiting IC failure initiates with thermal-stress-related crack formation where dielectric passivation layers overcoat micron-scale vertical features including patterned metal traces.

Introduction

Transistor integrated circuits (ICs) capable of prolonged reliable operation well above the effective 300 °C limit of silicon-on-insulator technology are expected to enable important improvements to aerospace, automotive, energy production, and other industrial systems [1,2]. NASA Glenn Research Center recently reported fabrication and initial testing of prototype 4H-SiC junction field effect transistor (JFET) integrated circuits (ICs) with two levels of interconnect that have consistently functioned for more than 1000 hours at 500 °C [3,4]. ICs from this same wafer have also been packaged using improved die-attach and tested to failure at 700 °C [5]. This report presents additional data and insights into the durability limits of this extreme temperature IC technology gained from further electrical testing and microscopic inspection of failed chips.

Experimental

The experimental details of design, fabrication, packaging, and oven-testing of the 4H-SiC JFET ICs are published elsewhere [3-6]. Figure 1 shows a cross-sectional scanning electron micrograph (SEM) of an as-fabricated JFET showing the two levels of patterned TaSi₂ metal interconnect embedded in dielectric [3,4]. Conformal coverage of metal and dielectric films over substantial topography seen in Fig. 1 is vital to realization of robust ICs, as are high-temperature durable contacts, bonding pads, die attach, and packaging [3-6]. Due to the non-trivial resources and challenge associated with initial prototype extreme-temperature packaging and testing, only a dozen chips from this wafer have undergone $T \geq 500$ °C durability testing to date. All oven durability testing was carried out in oxygen-containing room air, and temperature ramp rates to and from 500 °C were confined to 3 °C/minute or less.

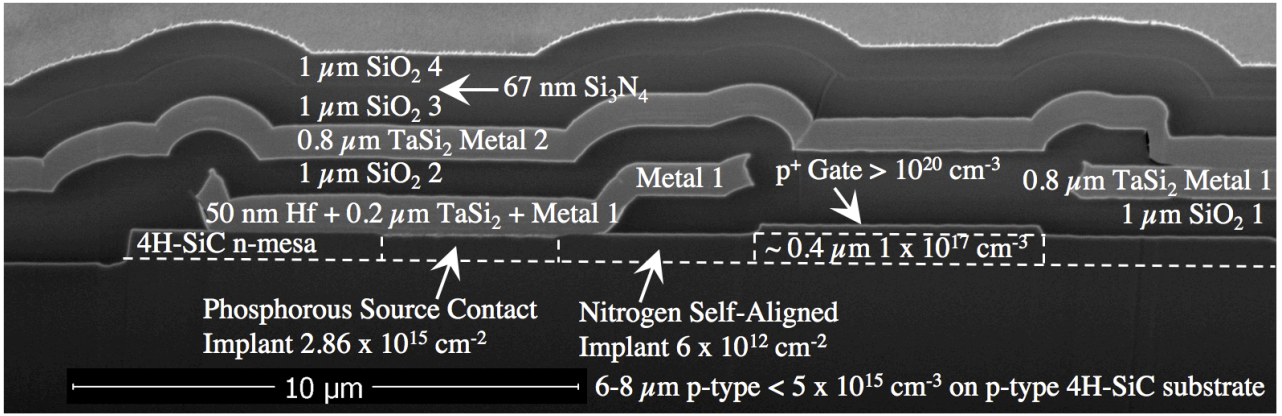


Figure 1. Annotated cross sectional micrograph of 4H-SiC JFET with two-layer interconnect [3]. The SiC JFET source and gate are shown, but the drain resides beyond the right edge of the image.

Results & Discussion

Electrical. Some circuits reported in [3,4] were still operating at 500 °C in prolonged oven-testing at the time of these prior publications. Updated final results of these 500 °C tests through failure of all circuits are shown in Figs. 2 and 3. As shown in Fig. 2, all three amplifier circuits failed between 4000 and 6500 hours of 500 °C testing time. Figure 3 shows that stable logic output was obtained from an medium frequency (MF) series NOT gate IC [3,4] for over 5000 hours at 500 °C prior to failure. Three other logic gates plotted in Fig. 3 failed much sooner, but none failed before 1900 hours of 500 °C testing [3,4].

Testing ICs at temperatures above the intended application temperatures is a common practice to more quickly reveal IC failure mechanisms. Towards this end, Figs. 4 and 5 show measured results from packaged chips that underwent such "accelerated" durability testing at 700 °C. Fig. 4 shows logic gate test waveforms from an MF series NOR logic gate [3-5] that operated for 142 hours at 700 °C prior to failure [3-5]. More complicated ring oscillator ICs also functioned at 700 °C but for less than 15 hours [5]. Figure 5 compares 700 °C output waveforms measured from 3-stage MF and high frequency (HF) design ring oscillators on the same chip. The nearly 2-fold difference in operating frequency is in agreement with the theoretically expected ratio arising from the 2-fold difference in the feedback ring NOT gate resistor values. These result demonstrate intrinsic 700 °C functionality of 4H-SiC JFET digital logic, even though extrinsic interconnect failure described below presently precludes long-term operation at this most extreme temperature.

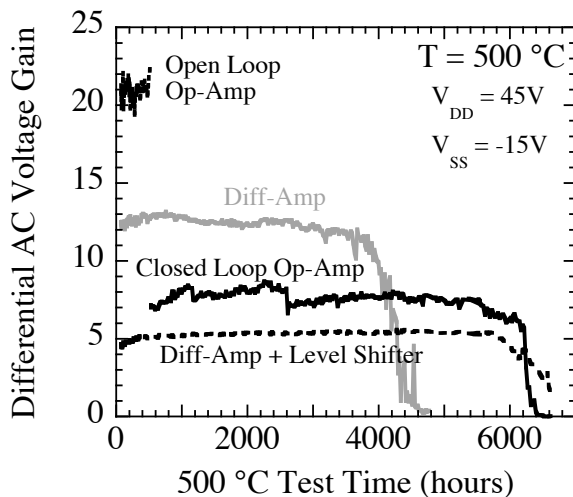


Fig. 2. Measured differential small-signal voltage gain vs. 500 °C amplifier testing time.

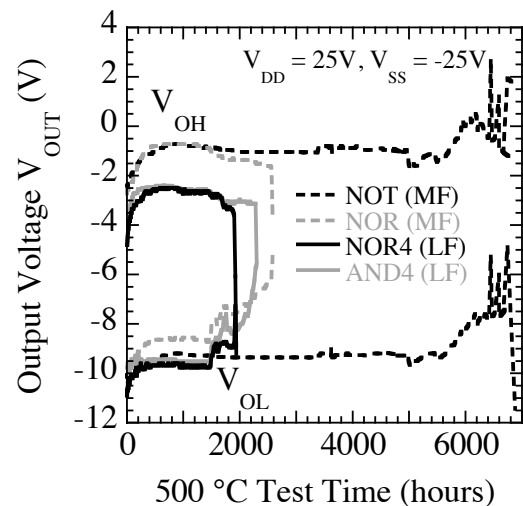


Fig. 3. Logic gate output high (V_{OH}) and output low (V_{OL}) voltages vs. 500 °C test time.

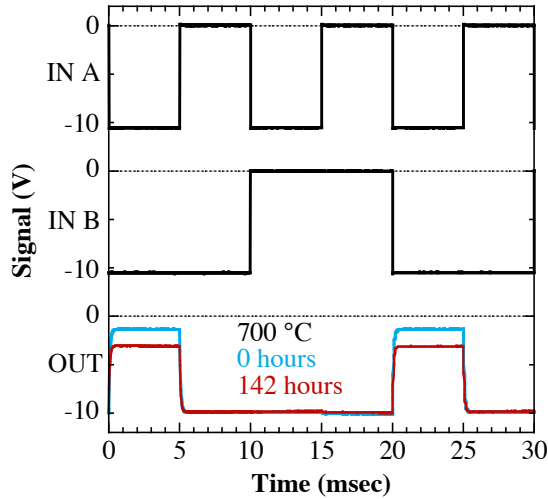


Fig. 4. NOR logic gate test waveforms measured at the start and 142 hours into 700 °C electrical testing.

Post-Failure Microscopic Observations.

500 °C Tested Chips. The three failed logic gates of Fig. 3 and a ring oscillator that failed at 1656 hours (all from the same chip) [3,4] have been microscopically examined. The failed circuits all exhibit observable dielectric film cracks associated with underlying TaSi₂ metal interconnect discoloration similar to what is evident in Fig. 6. Discoloration is present in both Metal 1 and Metal 2 layers, but the optical color contrast is more pronounced for Metal 2 traces. The cracks and discoloration are consistent with the SiC resistor failure reported in [4]. It was hypothesized in [4] that thermal-stress-related cracking of the overlying SiO₂/Si₃N₄/SiO₂ dielectric passivation occurs first, leading to subsequent penetration of atmospheric oxygen to the underlying TaSi₂ metallization, followed by metal oxidation leading to open-circuit failures of interconnects. The variations in 500 °C circuit lifetimes are surmised to arise from varying dielectric crack pattern evolution under biased circuit testing. As evidenced in Fig. 6, cracks often, but not exclusively, propagate along the edges of patterned metal features. Preferential dielectric film crack formation near surface topography imposed by metal edges is consistent with observations that wider metal traces are often discolored only near the edges of the metal pattern (e.g., upper right M2 trace of Fig. 6), whereas discoloration completely spans the length and width of narrower metal traces (e.g., 12 μm wide lower right M2 trace of Fig. 6).

700 °C Tested Chips. The far more extensive dielectric and metal film damage found in 700 °C tested chips is shown in Fig. 7. The SEM study elucidated cases where underlying Metal 1 traces apparently swelled in thickness to push up and extensively crack the overlying dielectric film. Oxidation of TaSi₂ at a crack site as well as bias effect on 700 °C interconnect degradation was reported in [5]. It is possible that after an initial dielectric crack forms

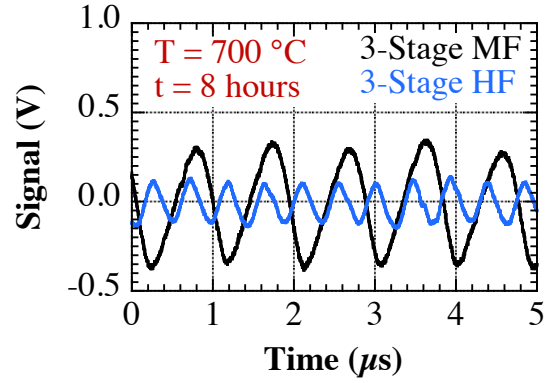


Fig. 5. Measured output waveforms of two different ring oscillator designs on the same packaged 3mm x 3mm SiC chip recorded 8 hours into 700 °C electrical testing. The MF design uses resistor values twice as large as the HF design, resulting in a ~2X frequency difference.

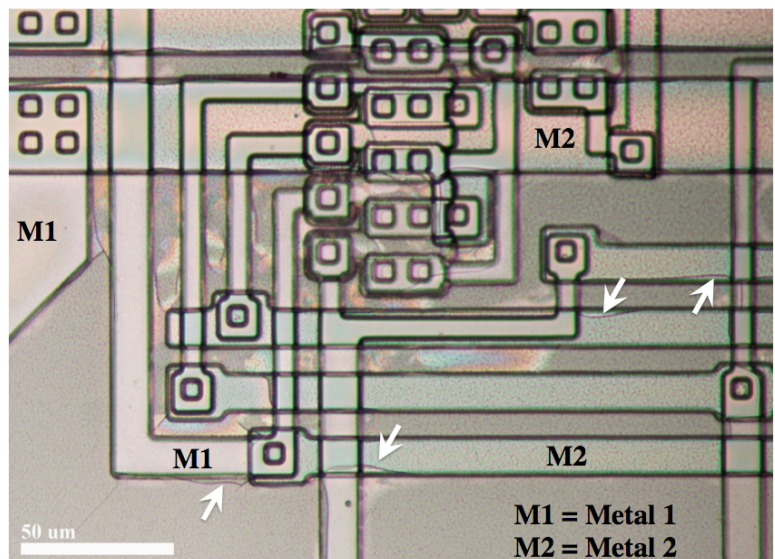


Fig. 6. Optical micrograph of part of the NOR4 logic gate that failed after 1916 hours of 500 °C testing, showing abundant dielectric cracks (some denoted by white arrows, many parallel to metal edges) and related discoloration of Metal 1 and Metal 2 traces.

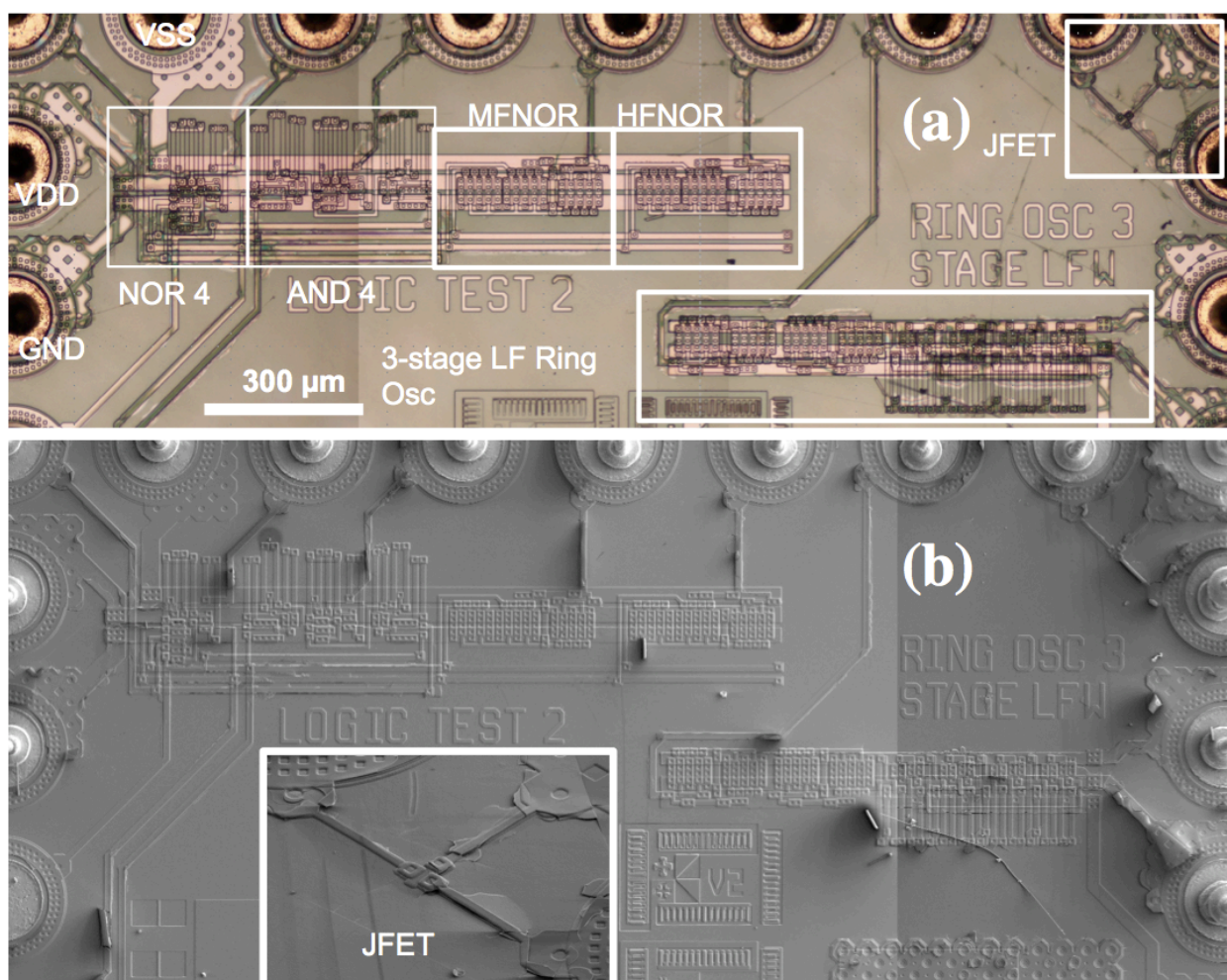


Fig. 7. (a) Optical [5] and (b) SEM images of the same chip region tested for 191.5 hours at 700 °C in air, documenting extensive dielectric and interconnect metal damage.

to permit oxidation of underlying metal, metal film oxidation causing an increase in volume (i.e., metal film swelling) might preferentially drive further dielectric crack propagation along metal film edges, eventually leading to the heaviest 700 °C testing damage observed for Metal 1 interconnects.

Conclusion

An unprecedented combination of $T \geq 500$ °C semiconductor IC durability and functionality has been demonstrated with high-temperature packaged chips from the latest generation two-level interconnect 4H-SiC JFET wafer. To further improve 500 °C operational lifetimes beyond a few thousand hours and/or increase operation to even higher temperatures, elimination or control of crack formation in the protective insulating dielectric films is necessary.

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